# Abstracts

## Automatic synthesis of a 2.1 GHz SiGe low noise amplifier

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A 2.1 GHz low noise amplifier in a 0.5 /spl mu/m 47 GHz SiGe BiCMOS process was synthesized and sent to fabrication. The circuit was synthesized to simultaneously meet multiple design specifications Including noise figure, gain, power, impedance match, intermodulation, compression, stability with a state-of-art simulation-based circuit synthesis tool. The synthesis setup took about two days, and the synthesis run took about 2 hours on a pool of 10 networked SUN workstations. Noise figure of 1.2 dB, power gain of 16 dB, IIP3 of -6 dB, S11 of less than -15 dB, were achieved with 3.7 mA bias current at 2.5 V power supply. Data generated during synthesis was processed to show design trade-offs among competing performance goals. The trade-off between optimum noise match and input impedance match Is discussed.

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